FORM PTO-1449 (SUBSTITUTE)

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE

INFORMATION DISCLOSURE STATEMENT BY APPLICANT
(37 CFR 1.98(b))

Attorney Docket No.:	Applic. No.
P2001,0158	10/657,928

Applicant: Wolfgang Gustin et al.

Filing Date	Group Art Unit
September 10, 2003	

U.S. PATENT DOCUMENTS

EXAMINER INITIALS		PATENT NO.	DATE	PATENTEE	CLASS	SUB CLASS	FILING DATE
	A						
	B						
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		DOCUMENT NO.	DATE	COUNTRY	CLASS	SUB CLASS	TRANSL. YES	TRANSL. NO
	J							
	K							
	L							
	M							
	N							

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

JSKS	O	L. Nesbit et al.: "A 0.6 μm² 256Mb Trench DRAM Cell With Self-Aligned BuriEd STrap (BEST)", *IEDM 1993, pp. 627-630*
JSKS	P	G. Bronner et al.: "A Fully planarized 0.25μm CMOS Technology for 256Mbit DRAM and Beyond", *1995 Symposium on VLSI Technology Digest of technical Papers, Kyoto, Japan, pp. 15-16*

EXAMINER	DATE CONSIDERED
JSKS	7/8/04

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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	L							
	M							
	N							

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

JKS	O	Stanley Wolf: "Silicon Processing For The VLSI Era – Volume 2: Process Integration", *Lattice Press, Sunset Beach, California, cover page only*
JKS	P	D. Widmann et al.: "Technologie hochintegrierter Schaltungen", *Springer Verlag, Heidelberg, Germany, 2nd ed., cover page only*

EXAMINER: [signature]

DATE CONSIDERED: 7/8/04

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OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

JKS	O	U. Gruening et al.: A Novel Trench DRAM Cell with a VERtIcal Access Transistor and BuriEd Strap (VERI BEST) for 4Gb/16Gb", *IEEE, 1999, 4 pp*
	P	

EXAMINER	DATE CONSIDERED
JKS	7/8/04

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EXAMINER INITIALS		PATENT NO.	DATE	PATENTEE	CLASS	SUB CLASS	FILING DATE
BKS	A	5,744,386	4/28/98	Kenney			
BKS	B	5,827,765	10/27/98	Stengl et al.			
BKS	C	5,670,805	9/23/97	Hammerl et al.			
BKS	D	5,360,758	11/1/94	Bronner et al.			
BKS	E	6,509,599 B1	1/21/03	Wurster et al.			
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		DOCUMENT NO.	DATE	COUNTRY	CLASS	SUB CLASS	TRANSL. YES	TRANSL. NO
BKS	J	196 20 625 C1	10/23/97	Germany				
BKS	K	100 45 694 A1	4/4/02	Germany				
BKS	L	0 971 414 A1	1/12/00	Europe				
BKS	M	00/35006	6/15/00	WIPO				
	N							

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

		Gruening, U. et al.: "A Novel DRAM Cell with a VERtical Access Transistor and BuriEd STrap (VERI BEST) for 4Gb/16Gb", IEEE, 1999, 4 pages

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BKS	7/8/04